Code No. 9193

FACULTY OF ENGINEERING

B.E. 4/4 (ECE) I - Semester (Main) Examination, December/January 2014-15

Subject : VLSI Design

Time : 3 Hours **Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.

PART – A (25 Marks)

1 What are the basic components of a verilog module? (2)
2 What is the difference between a gate instantiation and module instantiation? (2)
3 Distinguish between procedure and function declarations in verilog. (2)
4 Draw the synthesis process flowchart. (3)
5 Draw the basic pseudo nMOS inverter and give the relative merits and demerits of the same with respect to CMOS. (3)
6 State the significance of design rules. (2)
7 Draw the stick diagram of CMOS 2 input XOR gate. (3)
8 Write the expressions for Rise time, fall time and maximum signal frequency. (3)
9 Draw the schematic diagram of D-flip flop using Transmission gates. (2)
10 Draw the circuit diagram of six Transistor RAM Cell. (3)

PART – B (50 Marks)

11 (a) Differentiate blocking and non-blocking assignments with suitable examples. (4)
(b) Write a verilog code and its test bench for a 4-bit comparator. (6)

12 Explain briefly about FSM module Devleop a verilog code for melay model for 4 states. Assume present state, next state and output. (10)

13 (a) Explain the operation of n-channel Depletion mode MOSFET with neat diagrams and characteristic curves. (5)
(b) Derive the expression for pull up to pull down ratio of an NMOS inverter driven by another nMOS Inverter. (5)

14 (a) With suitable sketches explain the main steps that are followed in standard Si CMOS fabrication process. (6)
(b) Draw the Transmission Gate based XOR and XNOR circuits. (4)

15 (a) Draw the stick diagrams and Layouts of Transmission gate and two input NAND gate. (6)
(b) How to estimate Resistance and capacitance of a MOS Transistor? (4)

16 (a) Explain the operation of Manchester carry adder with neat diagrams. (5)
(b) Draw the logic diagram of 8-bit NOR based ROM and explain its operation. (5)

17 Write short notes on the following:
(a) carry skip adder (5)
(b) Continuous assignment and delays in dataflow modeling (5)

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