Very Large Scale Integration (VLSI)

Lecture 3

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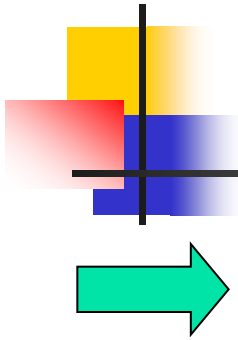
Contents

- Wiring tracks
- Latch-up
- Circuit characterization & performance
  - Resistance estimation
  - Capacitance estimation
  - Inductance estimation
- Delay estimation
  - Simple RC model
  - Penfield-Rubenstein Model
- Delay minimization techniques
  - Transistor sizing
  - Distributed drivers
  - Large driver
- Wiring techniques

Circuit characterization & performance



- Resistance estimation
- Capacitance estimation
- Inductance estimation

Parastic Elements

- So far, we've concentrated on getting circuit elements that we want for digital design
  - Transistors
  - Wires
- Parasitics - occur whether we want them or not
  - Capacitors
  - Resistors
  - Transistors (bipolar and FET)

Resistance estimation

- Resistance of uniform slab can be given as,

$$R = \frac{\rho}{t}.\frac{l}{w} \quad ohms$$

Where ρ = resistivity

t= thickness

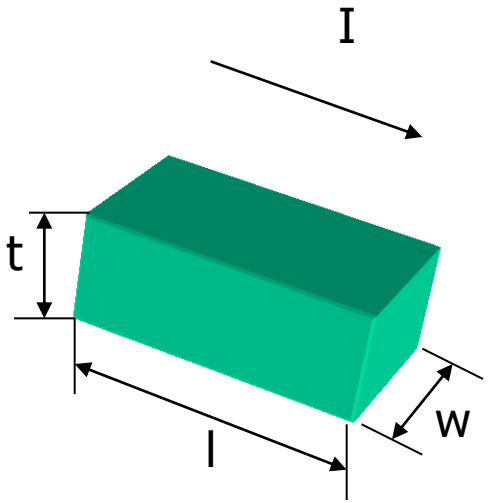
l= conductor length

w=conductor width

or,

$$R = R_s.\frac{l}{w} \quad ohms$$

R_s is the sheet resistance Ω/□



Resistance estimation (cont.)

- Resistance of certain layers

Material	R_s (Ω/□)
metal	0.03
Poly	15→100
Diffusion p	80
Diffusion n	35
Silicide	2→4
N-well	1K → 5K

Resistance estimation

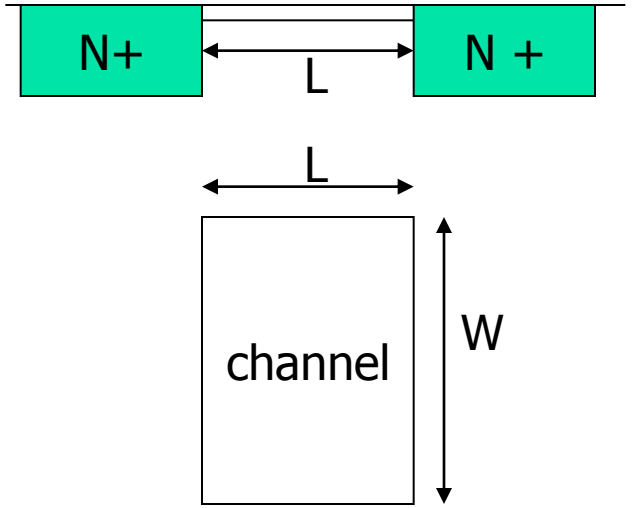
- For MOSFET channel resistance

$$R_{channel} = R_{Sheet}\,(L/W)$$

where $R_{sheet} = 1/\mu C_{OX}(V_{gs}-V_t)$

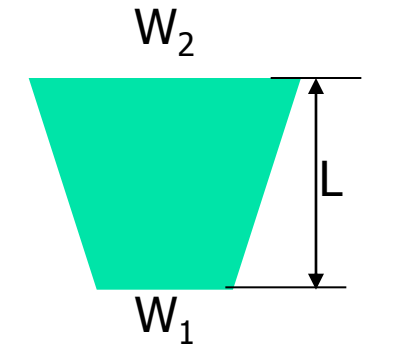
For P and n channels

$$R_{sheet} = 1000 \text{ ->} 30{,}000\ \Omega/\square$$

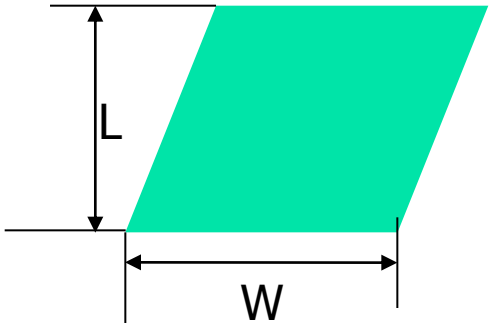


Resistance estimation (cont.)

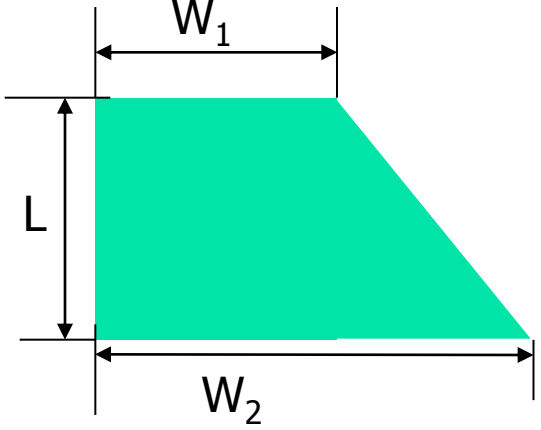
- Resistance of non rectangular regions



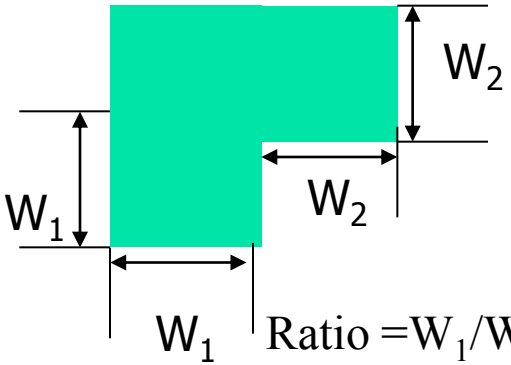
Ratio = $2L/(L+2W_1)$



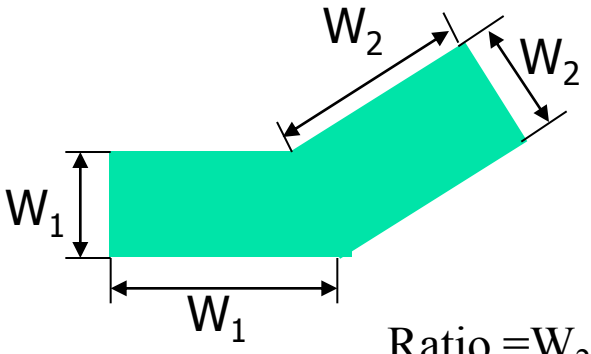
Ratio =L/W



Ratio =L/W



Ratio = W_1/W_2

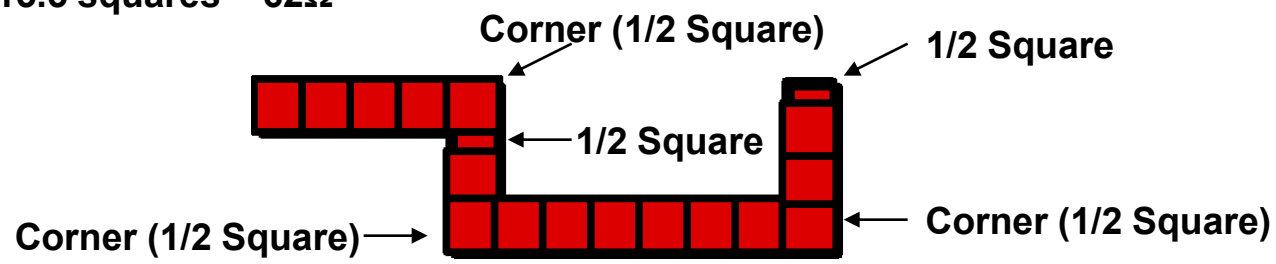


Ratio = W_2/W_1

Resistance

- Depends on resistivity of material ρ (Rho)
- Sheet resistance $R_s = \rho / t$
- Resistance $R = R_s * L / W$
- Corner approximation - count a corner as half a square

Example:
$R = R_{s(poly)} * 13 + 2*(1/2) + 3*(1/2)$ squares
$R = 4\Omega/sq * 15.5$ squares $= 62\Omega$



Inverter resistance estimation

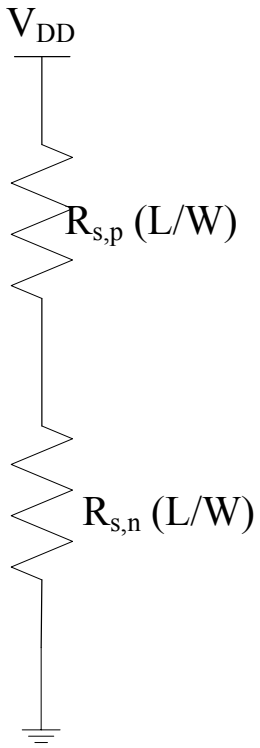
- CMOS inverter (no static current)
- Switching current

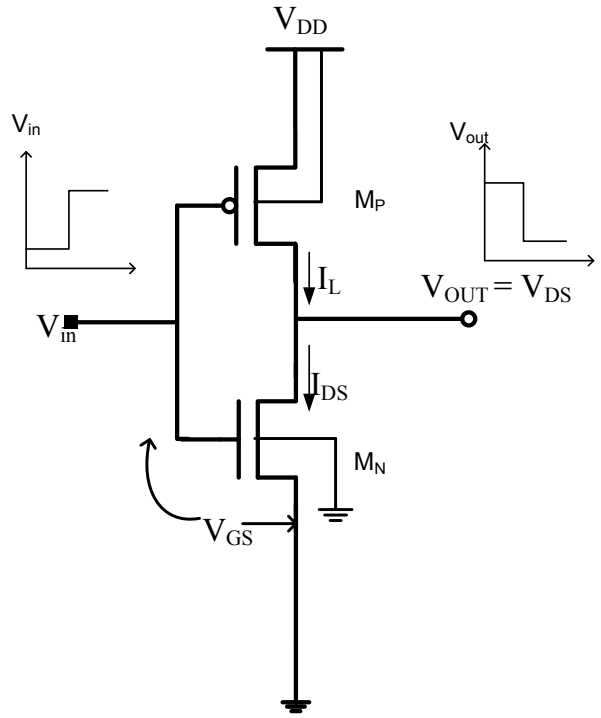
$$I_{\max} = \frac{V_{DD}}{R_{total}} = \frac{V_{DD}}{R_{s,p}\frac{L}{W} + R_{s,n}\frac{L}{W}}$$

$$for \qquad L = W = 1$$

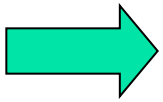
$$I_{\max} = \frac{V_{DD}}{R_{s,p} + R_{s,n}} = \frac{V_{DD}}{25+10} = \frac{V_{DD}}{35}$$

$$switching\ \ power\ \ loss = I_{\max}.V_{DD} = \frac{V_{DD}^2}{35}$$





Circuit characterization & performance

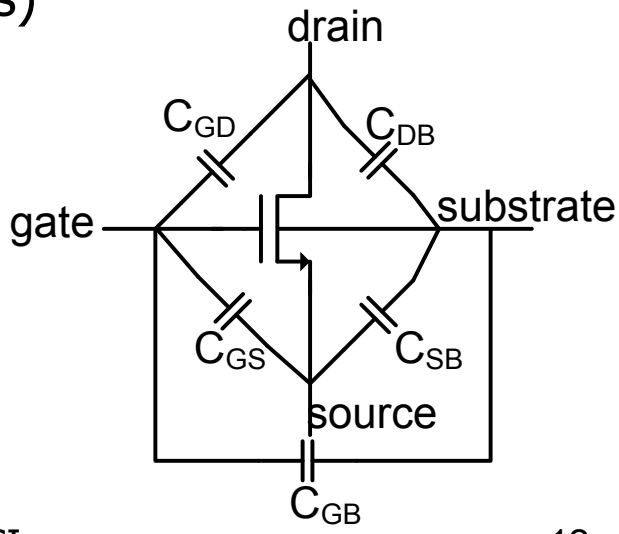


- Resistance estimation
- Capacitance estimation
  - Transistor capacitance
  - Routing capacitance
- Inductance estimation
- Delay estimation

Capacitance estimation

The dynamic response of MOS systems strongly depends on the parasitic capacitances associated with the MOS device. The total load capacitance on the output of a CMOS gate is the sum of:

- gate capacitance (of other inputs connected to out)
- diffusion capacitance (of drain/source regions)
- routing capacitances (output to other inputs)



Capacitance (1/2)

- Transistors
  - Depends on area of transistor gate
  - Depends on physical materials, thickness of insulator
  - Given for a specific process as C_g
- Diffusion to substrate
  - Side-wall capacitance - capacitance from periphery
  - bottom-wall capacitance - capacitance to substrate
  - Given for a specific process as $C_{diff,bot}$, $C_{diff,side}$

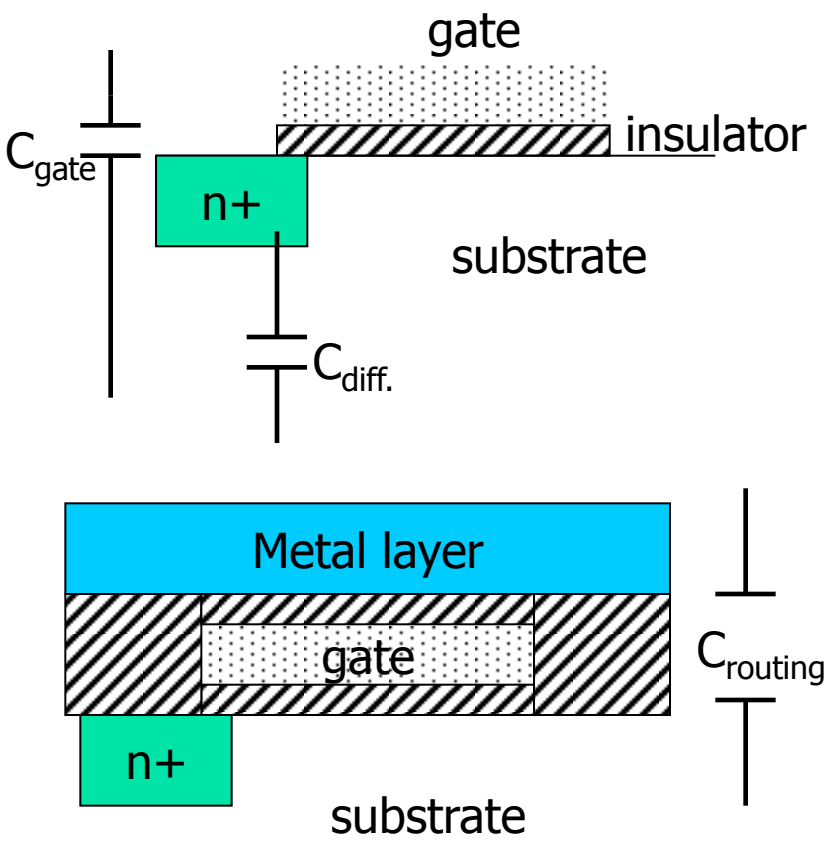
Capacitance (2/2)

- Metal to substrate
  - Parallel plate capacitance is dominant
  - Need to account for fringing, too
- Poly to substrate
  - Parallel plate plus fringing, like metal
  - don't confuse poly over substrate with gate capacitance
- Also important: capacitance between conductors
  - Metal1-Metal1
  - Metal1-Metal2

Capacitance estimation (cont.)

- Gate capacitance
- Diffusion capacitance
- Routing capacitance

- $C_{diff} > C_{poly} > C_{m1} > C_{m2}$

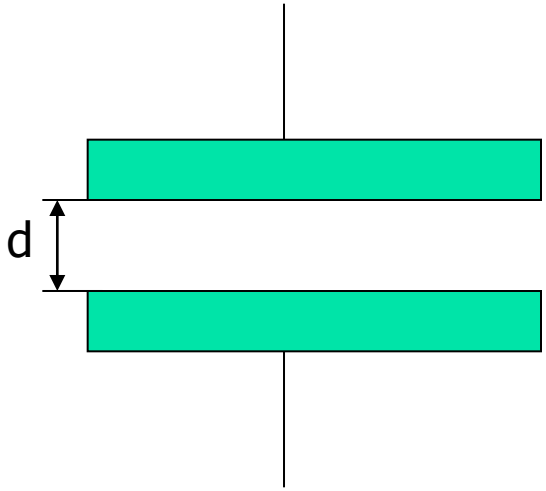


Capacitance estimation

- In general, capacitance could be calculated using

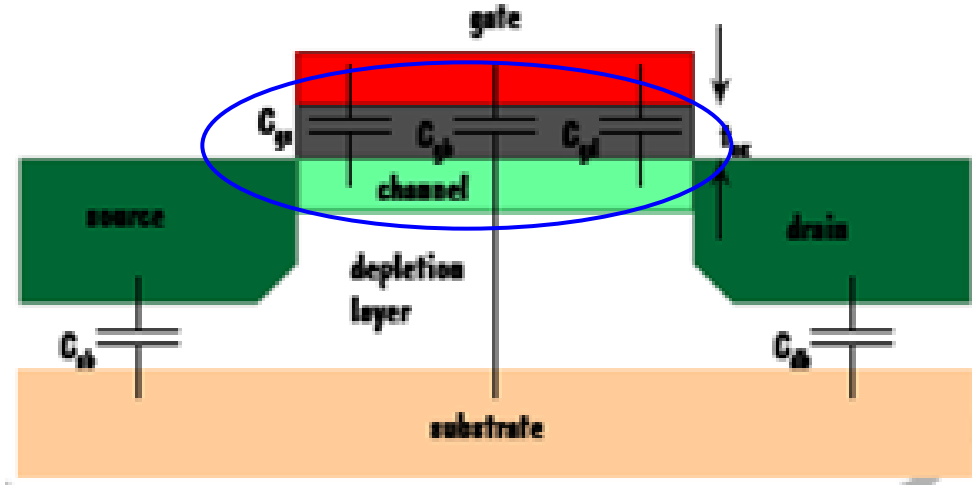
$$C = \frac{\varepsilon . A}{d} = \frac{\varepsilon_o . \varepsilon_r . A}{d}$$

$$C_{/unitarea} = \frac{\varepsilon_o . \varepsilon_r}{d} = C_{ox}$$



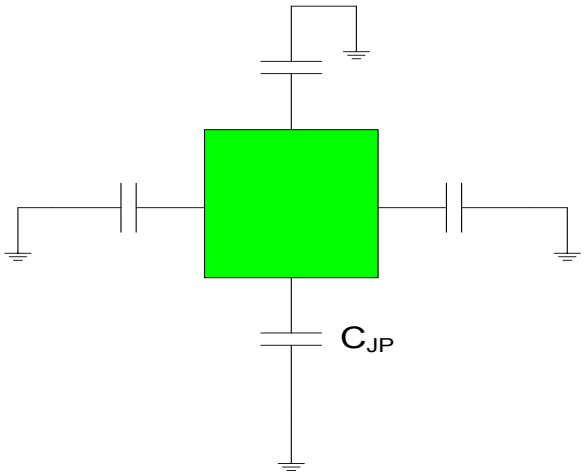
Gate Capacitance

- $C_g = C_{gs} + C_{gd} + C_{gb}$

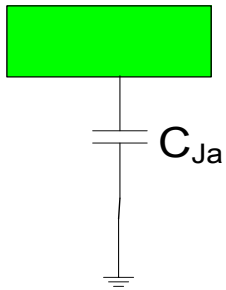


Capacitance estimation (cont.)

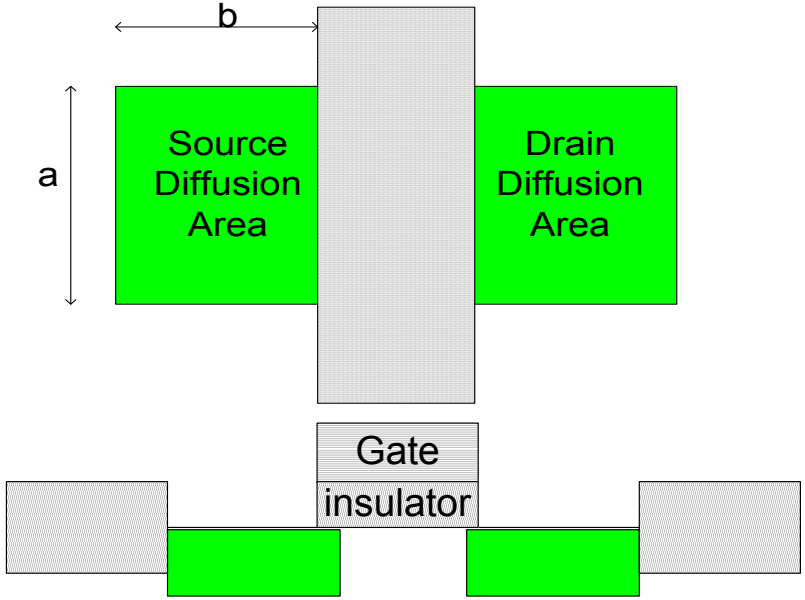
- Diffusion capacitance (source/drain)



Side wall capacitance

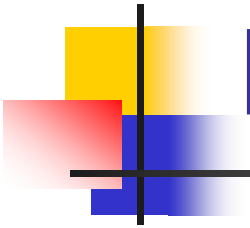


area capacitance



$$C_{s,diff} = C_{d,Area}.A + C_{d,sidewalls}.P$$

Where A = area and p = perimeters

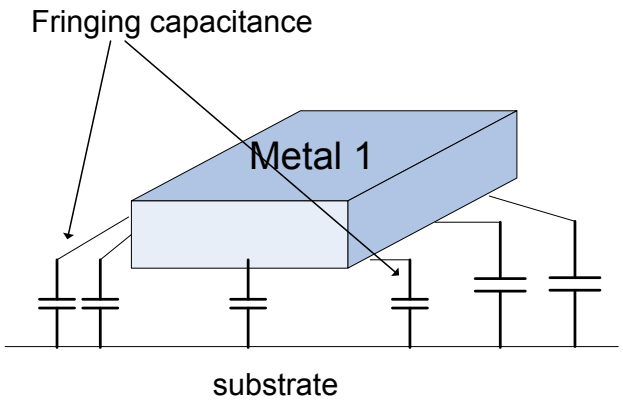


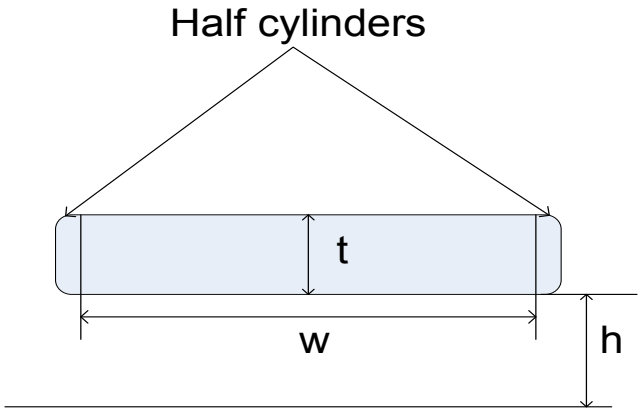
Routing capacitance

- single conductor capacitance
- multiple conductor capacitance

Capacitance estimation (cont.)

Routing capacitance: a) single conductor capacitance

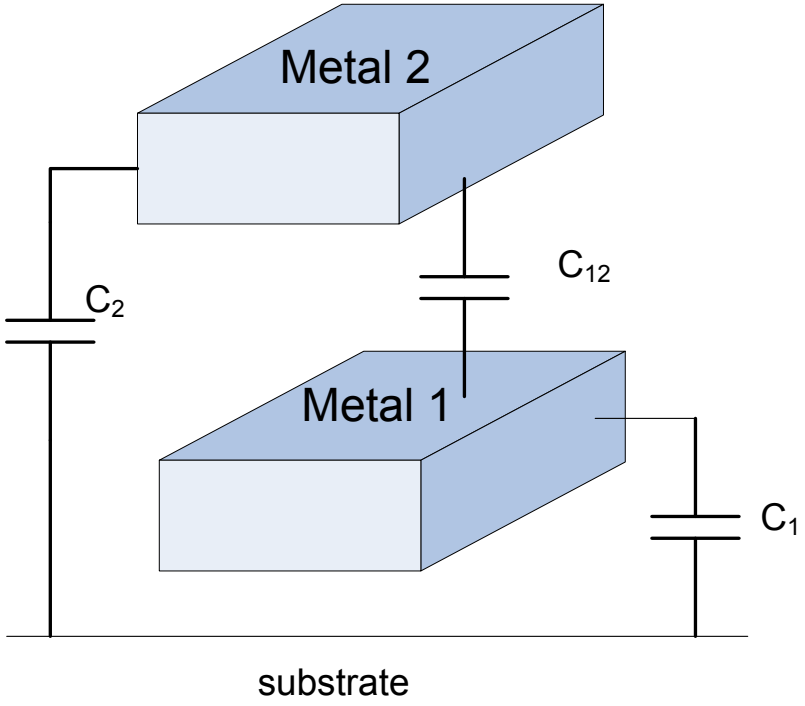


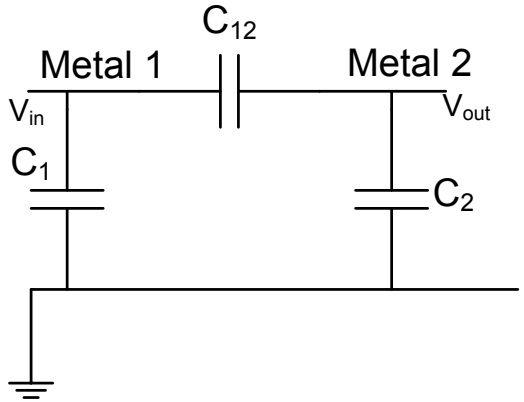


$$C_{total} = \varepsilon \left[\frac{w - \frac{t}{2}}{h} + \frac{2\Pi}{\ln\left[1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left[\frac{2h}{t} + 2 \right]} \right]} \right]$$

Capacitance estimation (cont.)

Routing capacitance: b) multiple conductor capacitance





$$\Delta V_{out} = \Delta V_{in} \cdot \frac{C_{12}}{C_2 + C_{12}}$$

Multilayer capacitance calculations

- Example: given the layout shown in the figure calculate the total capacitance at source and gate given that:

$C_{metal/Area} = 0.025\mu F/\mu m^2$

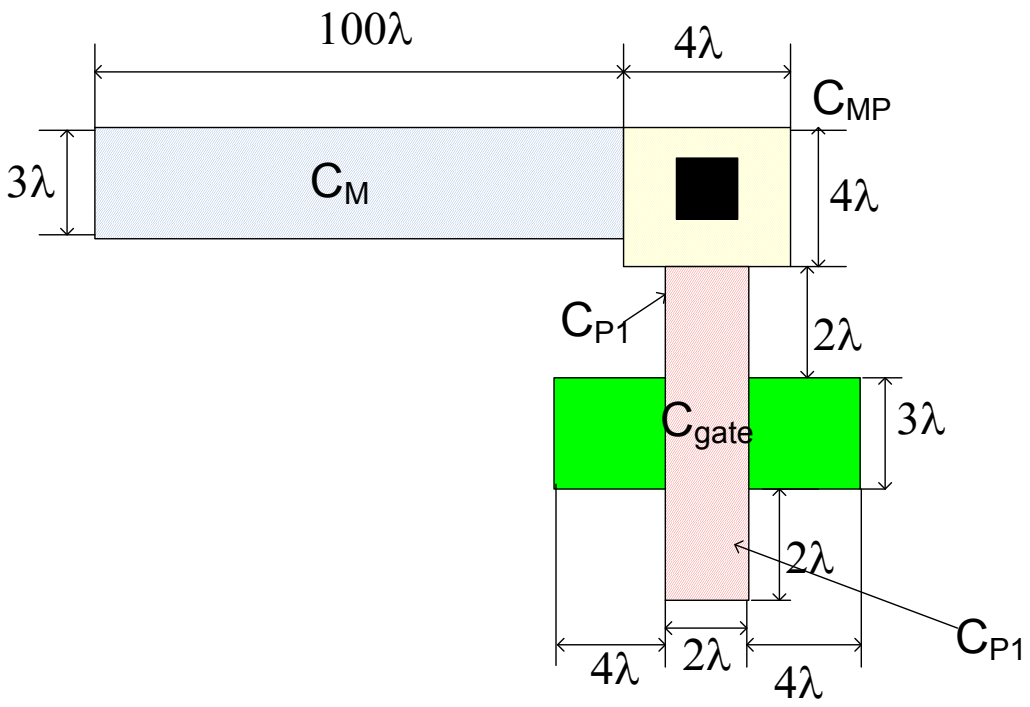
$C_{poly/Area} = 0.045\mu F/\mu m^2$

$C_{Gate/A} = 0.7\ fF/\mu m^2$

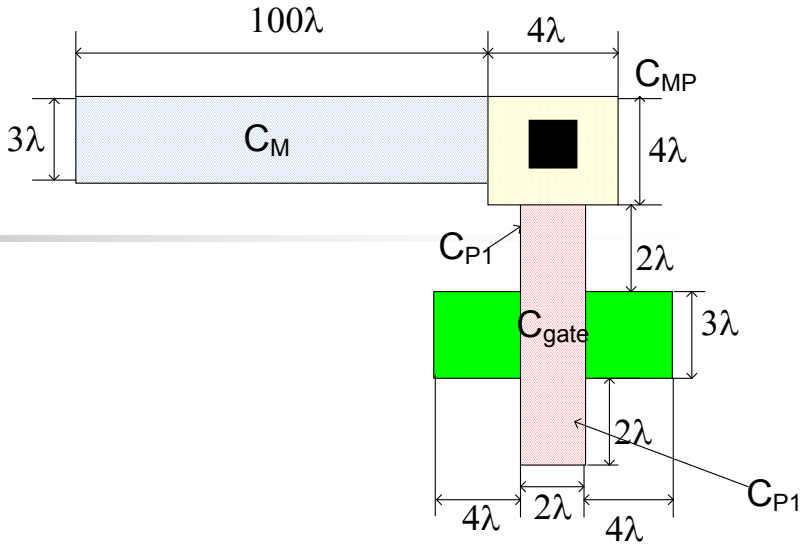
$C_{d,a/A} = 0.33fF/\mu m^2$

$C_{d,side/L} = 2.6fF/\mu m$

$\lambda = 5.1\mu m$



Solution



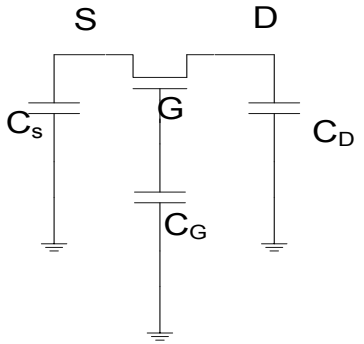
Source capacitance

$$C_{S,diff} = C_{d,A} \cdot A + C_{d,side\ walls} \cdot P$$

$$A = 4\lambda * 3\lambda = 12\ \lambda^2$$

$$P = 2*(4\lambda + 3\lambda) = 14\ \lambda$$

So, $C_{S,\ diff} = 0.33*\ 12\ \lambda^2 + 2.6*\ 14\ \lambda = 63.51 fF$



Solution (cont.)

Gate capacitance

$$C_{G,total} = C_M + C_{MP} + C_{P1} + C_G + C_{P2}$$

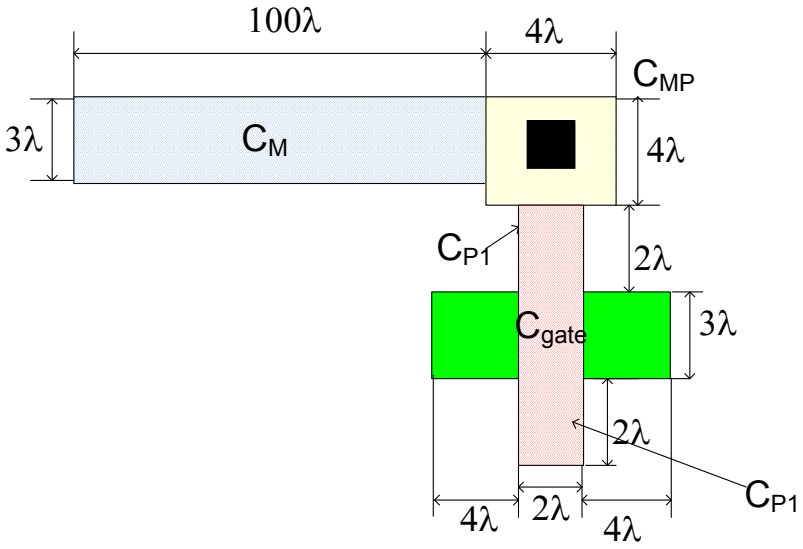
$$C_M = 0.025 * 100\lambda * 3\lambda = 7.5\lambda^2$$

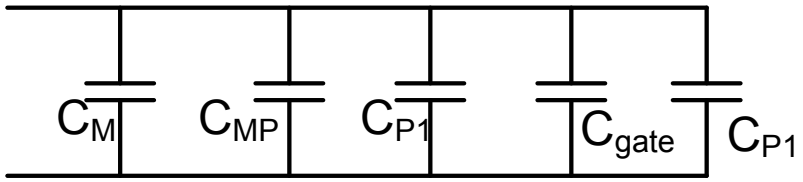
$$C_{MP} = 0.045 * 4\lambda * 4\lambda = 0.72\lambda^2$$

$$C_{P1} = 0.045 * 2\lambda * 2\lambda = 0.18\lambda^2$$

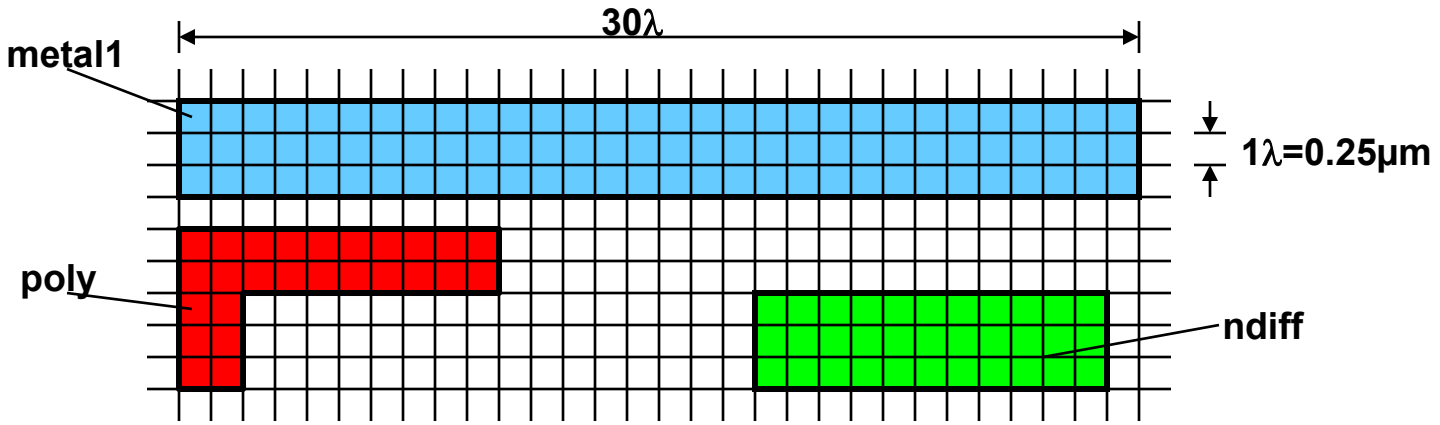
$$C_{P2} = 0.045 * 2\lambda * 2\lambda = 0.18\lambda^2$$

$$C_G = 0.7 * 2\lambda * 3\lambda = 4.2\lambda^2$$





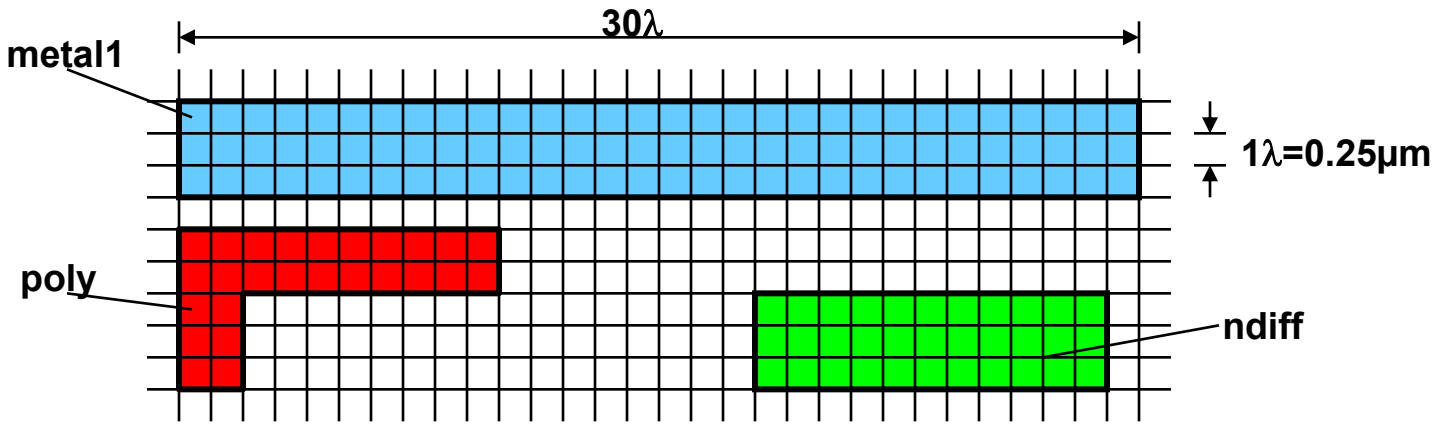
Example Problems - Parasitic Calculation (1/10)



Rmetal1=? **Rpoly=?** **Rndiff=?**

Cmetal1=? **Cpoly=?** **Cndiff=?**

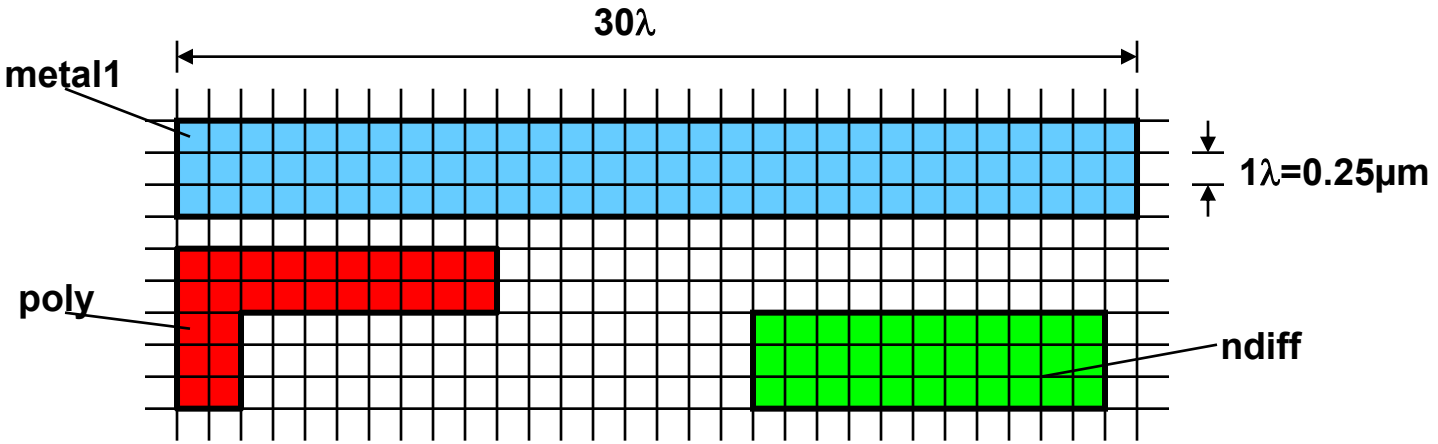
Example Problems - Parasitic Calculation (2/10)



$$R_{metal1} = (30\lambda / 3\lambda) * 0.08\Omega/\square = 0.8\Omega$$

$$C_{metal1} = (30\lambda * 0.25\mu m/\lambda) * (3\lambda * 0.25\mu m/\lambda) * 0.04fF/\mu m^2 + (30\lambda + 3\lambda + 30\lambda + 3\lambda) * 0.25\mu m/\lambda * 0.09fF/\mu m$$
$$= 0.225fF + 1.485fF$$
$$= 1.71fF$$

Example Problems - Parasitic Calculation (3/10)



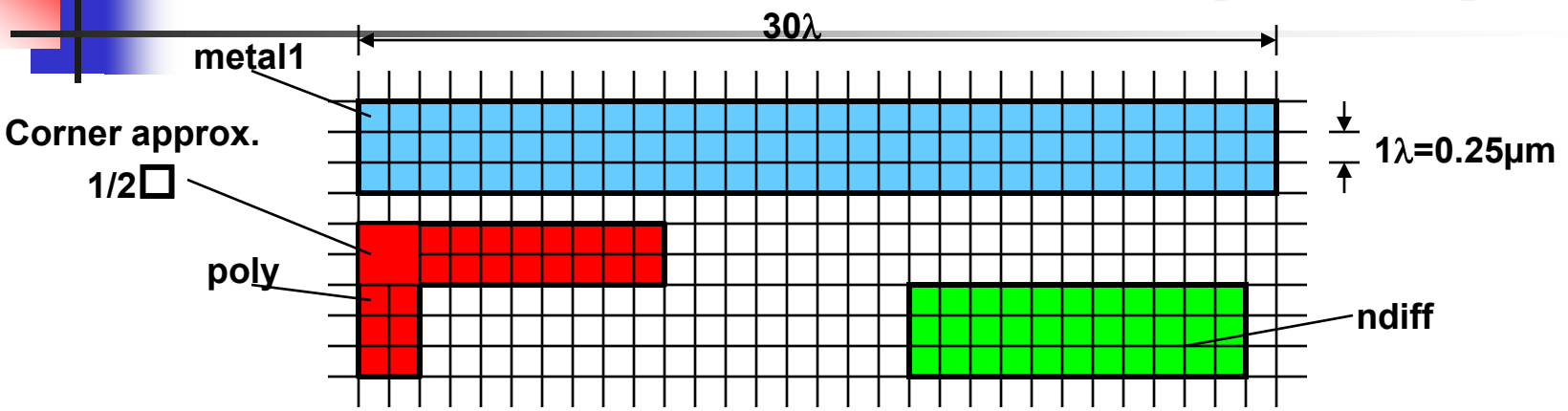
$$Rndiff = (11\lambda / 3\lambda) * 2\Omega/\square = 7.33\Omega$$

$$Cndiff = (11\lambda * 0.25\mu m/\lambda) * (3\lambda * 0.25\mu m/\lambda) * 0.6fF/\mu m^2 + (11\lambda + 3\lambda + 11\lambda + 3\lambda) * 0.25\mu m/\lambda * 0.2fF/\mu m$$

$$= 1.24fF + 1.4fF$$

$$= 2.64fF$$

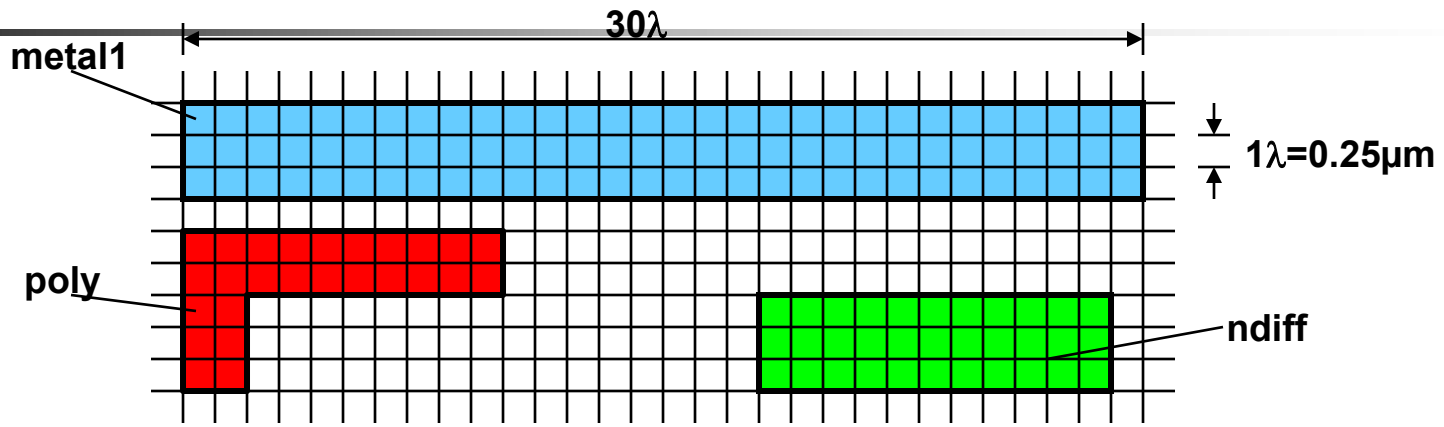
Example Problems - Parasitic Calculation (4/10)



$$R_{poly} = ((3\lambda / 2\lambda) + 1/2\square + (8\lambda / 2\lambda)) * 4\Omega/\square = 24\Omega$$

$$C_{poly} = (((3\lambda * 0.25\mu m/\lambda) * (2\lambda * 0.25\mu m/\lambda)) + ((10\lambda * 0.25\mu m/\lambda) * (2\lambda * 0.25\mu m/\lambda))) * 0.09fF/\mu m^2 + (5\lambda + 10\lambda + 2\lambda + 8\lambda + 3\lambda + 2\lambda) * 0.25\mu m/\lambda * 0.04fF/\mu m$$
$$= 0.15fF + 0.3fF$$
$$= 0.45fF$$

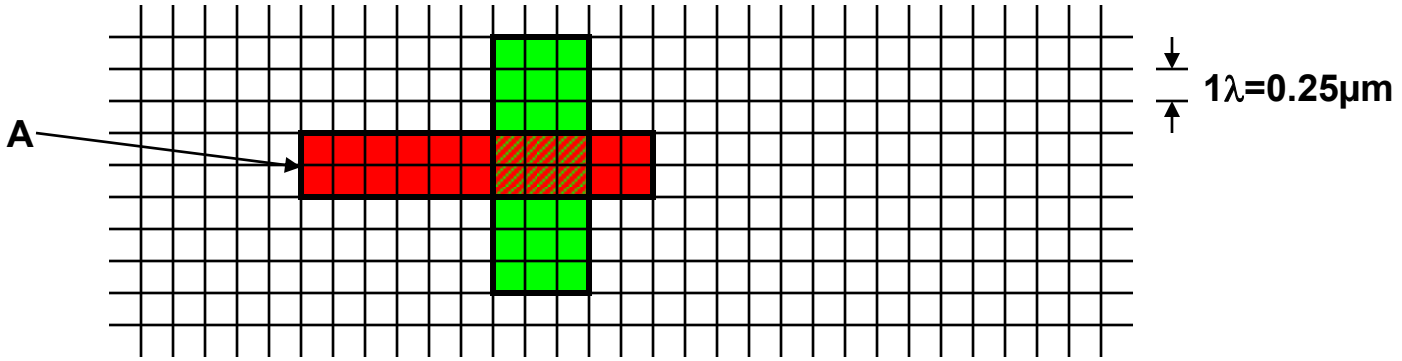
Example Problems - Parasitic Calculation (5/10)



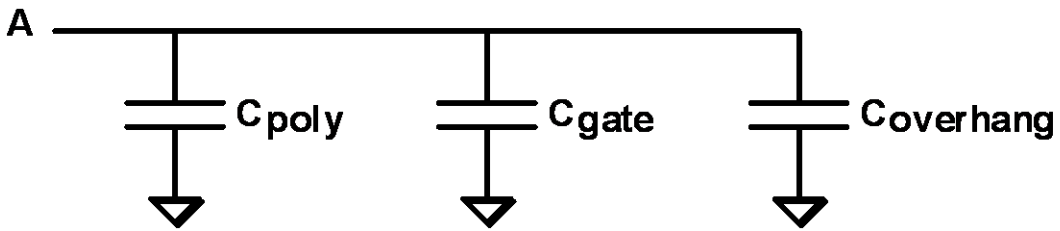
Rmetal1=0.8Ω **Rndiff=7.33Ω** **Rpoly=24Ω**

Cmetal1= 1.71fF **Cndiff= 2.64fF** **Cpoly= 0.45fF**

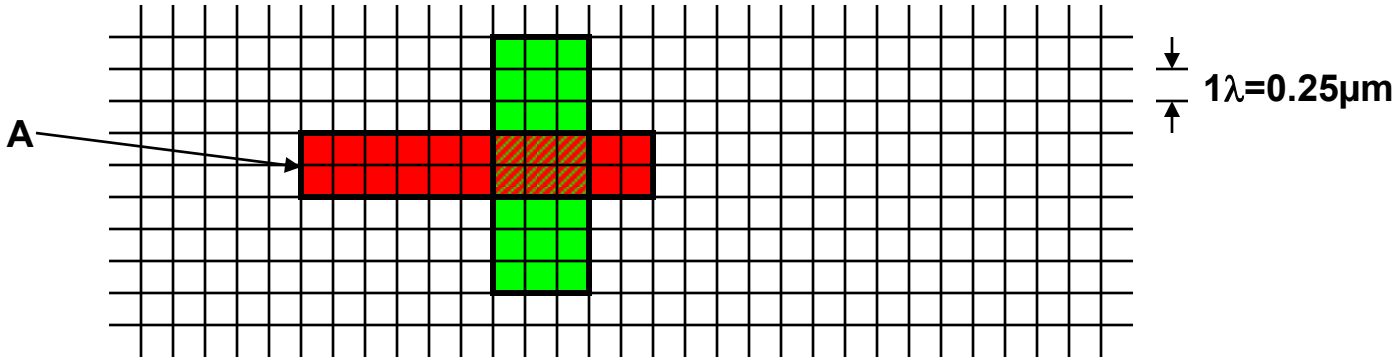
Example Problems - Parasitic Calculation (6/10)



What are the parasitic capacitances visible from point "A"?



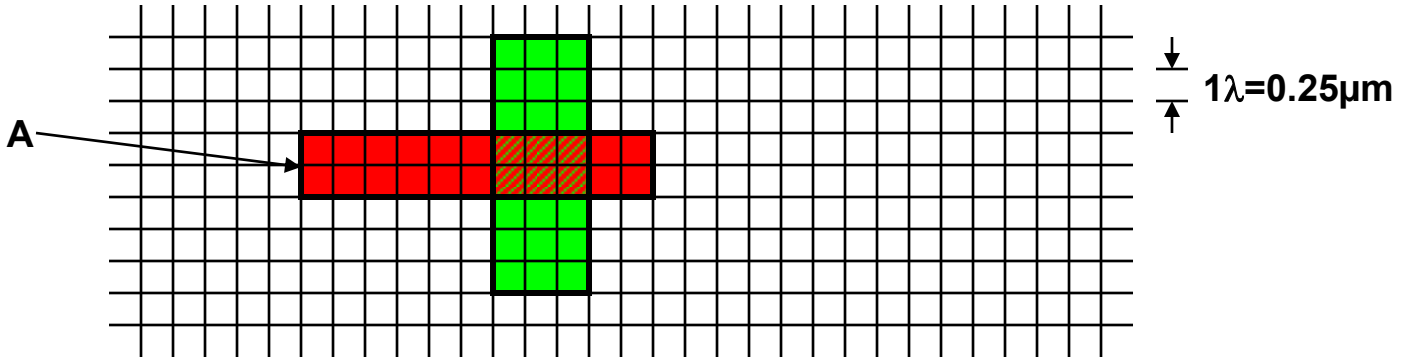
Example Problems - Parasitic Calculation (7/10)



What are the parasitic capacitances visible from point "A"?

$$\begin{aligned} C_{poly} &= (6\lambda * 0.25\mu m/\lambda) * (2\lambda * 0.25\mu m/\lambda) * 0.09fF/\mu m^2 + \\ &\quad (6\lambda + 2\lambda + 6\lambda + 2\lambda) * 0.25\mu m/\lambda * 0.04fF/\mu m \\ &= 0.675fF + 0.16fF \\ &= 0.84fF \end{aligned}$$

Example Problems - Parasitic Calculation (8/10)

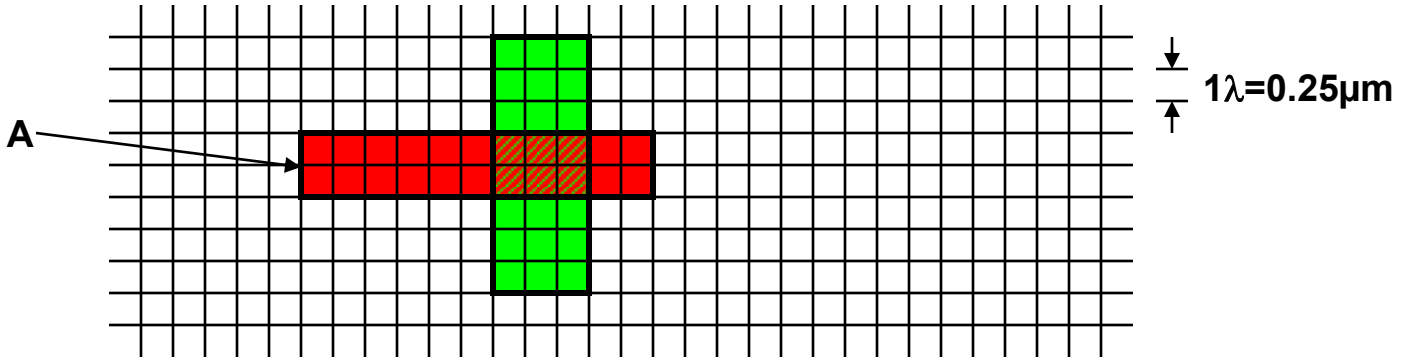


What are the parasitic capacitances visible from point "A"?

$$C_{gate} = (3\lambda * 0.25\mu m/\lambda) * (2\lambda * 0.25\mu m/\lambda) * 0.9fF/\mu m^2$$
$$= 0.34fF$$

Remember: use Cg, not Cpoly for transistor gates!

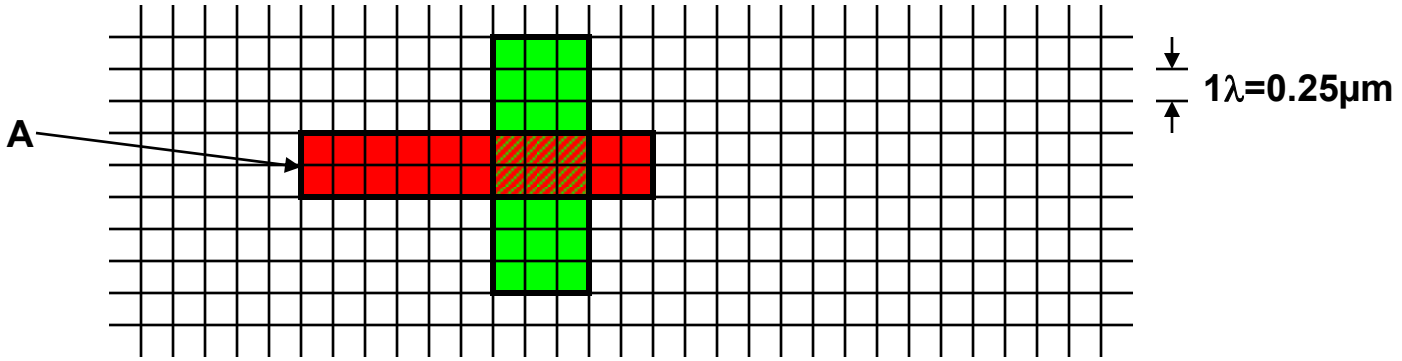
Example Problems - Parasitic Calculation (9/10)



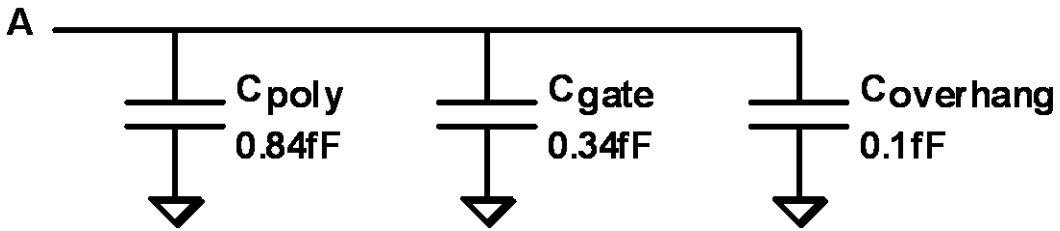
What are the parasitic capacitances visible from point "A"?

$$C_{overhang} = (2\lambda * 0.25\mu m/\lambda) * (2\lambda * 0.25\mu m/\lambda) * 0.09fF/\mu m^2 + (2\lambda + 2\lambda + 2\lambda + 2\lambda) * 0.25\mu m/\lambda * 0.04fF/\mu m$$
$$= 0.0225fF + 0.08fF$$
$$= 0.1fF$$

Example Problems - Parasitic Calculation (10/10)



What are the parasitic capacitances visible from point "A"?



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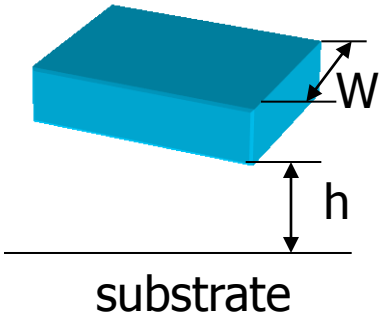
Inductance estimation

- Inductance is normally small but as the process shrink on-chip inductance must be taken into account.
- Bond-wire inductance can cause deleterious effects in large, high speed I/O buffers.
- The inductance of bonding wires and the pins on packages could be calculated by,

$$L = \frac{\mu}{2\Pi} \ln\left(\frac{8h}{w} + \frac{4h}{d}\right)$$



Design techniques to overcome this problem:

- ✓separate power pins for I/O pads and chip core
- ✓multiple power and ground pins
- ✓careful selection of the position of the power and ground pins on the package
- ✓adding decoupling capacitances on the board
- ✓increase the rise and fall times
- ✓use advanced package technologies (SMD, etc)